Bidirectional Fast Charging Management Chip CH227

Datasheet

Version: 1.4

https://wch-ic.com

1. Overview

The CH227 series chips are bidirectional fast charging management chips designed for simultaneous charging and discharging via a Type-C interface USB connection.

The CH227F single-chip integrates the USB PD3.2 protocol, supporting data role, power role switching, and fast role exchange. It supports dual-port data packet transparent transmission and supports a maximum charging power of 140W in EPR mode. The CH227F features an integrated high-voltage LDO, offering low static power consumption, high integration, and simplified peripheral circuits. It supports firmware upgrades via the Type-C interface. Additionally, the CH227F incorporates an N-channel MOSFET power transistor gate boost driver module, capable of driving multiple high-side NMOS transistors to enable power path switching control.

The CH227P single-chip integrates the USB PD2.0 protocol, supports a maximum charging power of 100W.

The CH227 series chips can be widely used in mobile phones, tablets, laptops, and other Type-C charging port expansion USB devices that require charging.

2. Function Features

- Support Data Role Swap (DR_Swap) on the host-side Type-C port.
- Support Power Role Swap (PR_Swap) on the host-side Type-C port.
- Support Fast Role Swap (FR_Swap) on the host-side Type-C port.
- Support PD3.2 fast charging protocol and EPR 140W power.
- Support reversible plug detection for Type-C female connectors on the host and power supply sides.
- Support PD fast charging protocol forwarding on the host and power supply sides.
- Support power reservation function, with a default reservation of 15W power.
- Bidirectional power supply with independent NMOS switch control, no voltage drop when conducting
- High integration on a single chip, simplified peripheral components, low cost
- Built-in high-voltage LDO, integrated overvoltage protection

3. Pinouts

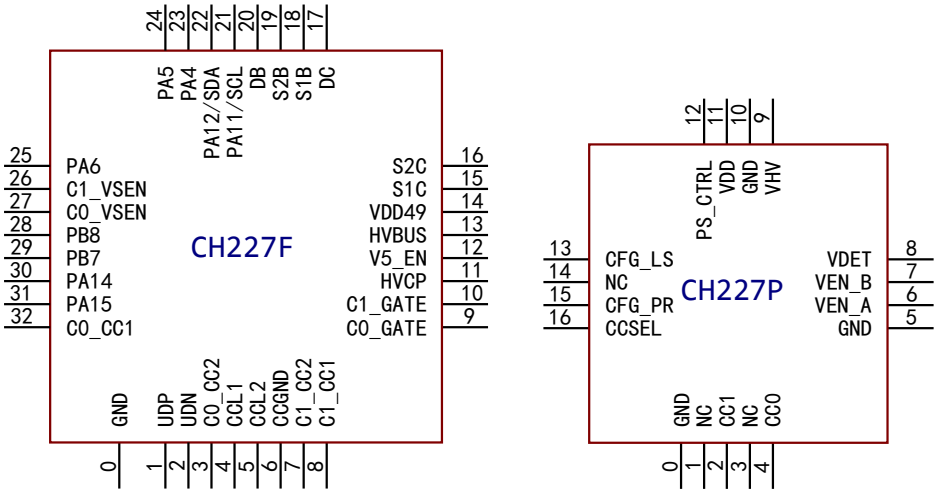


Table 3-1 Package description

Package form	Body size	Pin pitch		Package description	Order model
QFN32	4.0*4.0mm	0.4mm	15.7mil	Quad Flat No-Lead Package	CH227F
QFN16	3.0*3.0mm	0.5mm	19.7mil	Quad Flat No-Lead Package	CH227P

Note: 1. Pin 0 refers to the EPAD of the QFN32 or QFN16 package.

2. For new designs, CH227F is recommended as it requires fewer peripheral components and has a low N-channel conduction resistance.

4. Pins Definitions

Table 4-1 CH227F pin definitions

Pin No. CH227F	Pin name	Pin type(1)	Pin description
0	GND	P	Common ground.
13	HVBUS	P, HV	Working power supply input, at least externally connected with 1uF capacitance to ground.
14	VDD49	P	Internal 4.9V regulator LDO output, external 1uF capacitor to ground.
11	HVCP	P, HV	High voltage output of boost module; The external ground is connected with 0.1uF 50V capacitor.
10	C1_GATE	I/O, HV	Used to drive the NMOS gate of the host-side high-side power path; 750K pull-up resistor required to HVCP pin.
9	C0_GATE	I/O, HV	Used to drive the NMOS gate of the supply terminal high-side power path; requires a 750K pull-up resistor to the HVCP pin.
6	CCGND	P	Auxiliary power supply, need to connect GND.
32	C0_CC1	I/O, Rd	Used for power supply terminal PD protocol communication.
3	C0_CC2		Used for power supply terminal PD protocol communication.
8	C1_CC1	I/O, Rd	Used for host-side PD protocol communication.
7	C1_CC2		Used for host-side PD protocol communication.
4	CCL1	I/O	PD protocol communication internal pin, should be connected to CCL2.
5	CCL2	I/O	Used for host-side PD protocol communication.
26	C1_VSEN	I	Used for host terminal power supply voltage detection.
27	C0_VSEN	I	Used for voltage detection of power supply terminal.
1	UDP	I/O	Used for power supply BC protocol handshake.
2	UDN	I/O	Used for power supply BC protocol handshake.
20/17	DB/DC	A	Common terminal of the 2-to-1 analog switch.
18/15	S1B/S1C	A	1 #terminal of the 2-to-1 analog switch.
19/16	S2B/S2C	A	2 #terminal of the 2-to-1 analog switch.
21	PA11/SCL	I/O/A	2-wire serial interface clock input, customized function.
22	PA12/SDA	I/O/A	2-wire serial interface data input and output, customized function.
12	V5_EN	I/O, HV	Used for USB device power supply control pin.
23	PA4	I/O, LV	General-purpose input and output pins.
24	PA5	I/O, LV	General-purpose input and output pins.
25	PA6	I/O, LV	General-purpose input and output pins.
28	PB8	I/O, LV	General-purpose input and output pins.
29	PB7	I/O, LV	General-purpose input and output pins.
30	PA14	I/O, LV	General-purpose input and output pins.
31	PA15	I/O, LV	General-purpose input and output pins.

Table 4-2 CH227P pin definitions

Pin No. CH227P	Pin name	Pin type(1)	Pin description
0,5,10	GND	P	Common ground.
9	VHV	P, HV	High voltage positive power input terminal, need external 1uF decoupling capacitor.
11	VDD	P	Internal power regulator LDO output, external 1uF decoupling capacitor.
2	CC1	I/O, Rd	Used for power supply terminal PD protocol communication.
4	CC0	I/O, Rd	Used for host terminal PD protocol communication.
6	VEN_A	I/O, HV	Control the power switch A between the host terminal and the power supply terminal.
7	VEN_B	I/O, HV	Control the power switch B between the host terminal and the power supply terminal.
8	VDET	I	Check power connection at power supply terminal.
12	PS_CTRL	I/O, HV	USB device power supply control pin.
13	CFG_LS	I	Power distribution configuration pin.
15	CFG_PR	I	Maximum output power configuration pin.
16	CCSEL	O	Power supply side Type-C reversible plug detection switch control pin
1,3,14	NC	-	Pin not defined, need to float.

Note 1: Pin type abbreviations explained:

I = TTL/CMOS level Schmitt trigger input, supporting input voltages in the VDD/VDD49 voltage range;

O = CMOS level 3-state output, supporting output voltages in the VDD/VDD49 voltage range;

P = Power supply;

HV = High-voltage drive pin, VBUS rated 4V to 28V, HVCP, C0_GATE, C1_GATE rated 4V ~ 36V;

LV = Low-voltage drive pin, supporting input and output within the VDD49 voltage range;

Rd = Built-in controllable Rd pull-down resistor defined by the Type-C specification, usable for the PD power-receiving end;

A = Analog signal input or output, supporting the VDD49 voltage range.

5. Function Description

5.1 Overview

The CH227F chip's host-side Type-C port supports DRP role switching. The power supply side and host-side Type-C ports support bidirectional transparent transmission of PD charging data packets, with a maximum support of PD3.2 EPR 140W (28V/5A) power. The host-side USB port is typically used in conjunction with the CH334 series of USB HUB chips, and the CH334 downstream can expand to support more USB devices.

5.2 HVBUS/VDD49 Pins

The HVBUS pin serves as a high-voltage input power pin, with a built-in high-voltage LDO generating low voltage output via the VDD49 pin. The HVBUS pin requires an external 1uF 50V decoupling capacitor connected to ground, with a working voltage range of 5-28V.

The VDD49 pin serves as both the output terminal of the high-voltage LDO and the internal working power input terminal, requiring an external 1uF decoupling capacitor connected to ground.

5.3 HVCP Pin

The HVCP pin generates a higher voltage based on HVBUS, increasing the voltage value VCP to approximately twice VDD49 minus 2V, which is used to control the gate of the external N-type MOSFET power transistor. It is recommended to connect an external 100nF capacitor.

5.4 GATE Pin

The C0_GATE and C1_GATE pins are both high-voltage open-drain pins and require an external pull-up of 750K to the HVCP pin, while also connecting to the gate of an external N-type MOSFET power transistor.

5.5 CC1/CC2, VSEN Pins

CH227F provides 2 sets of CC pins for the host-side and power supply side. The C1_CC1 and C1_CC2 pins are used to implement PD protocol communication with host-side devices, supporting power and data role switching and fast role switching. The C0_CC1 and C0_CC2 pins are used to implement PD protocol communication with power supply-side adapters, supporting SPR and EPR, with a maximum support for EPR 28V communication.

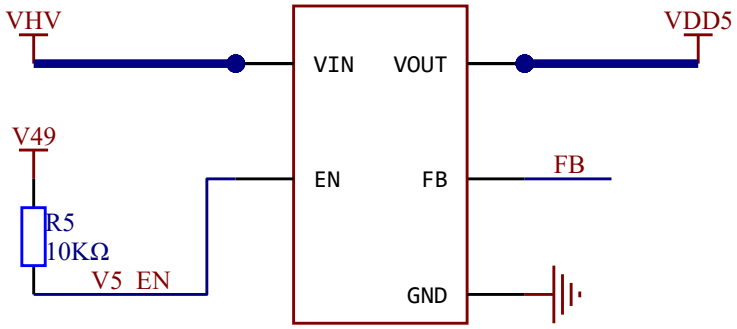
The C0_VSEN and C1_VSEN pins are used to detect the input voltage of the power supply side and host-side, with a resistor voltage division ratio of 25:3, using 150K/18K voltage division resistors. The CCL1 and CCL2 pins should be connected to each other, and the CCGND pin should be connected to GND.

5.6 V5_EN Pin

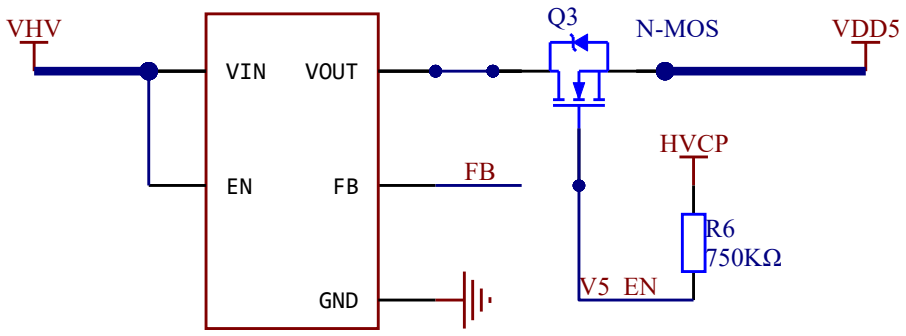
The USB device power supply control pin of CH227F. Some USB devices cannot resume communication when DR_SWAP occurs. This pin can be used to control the power supply on/off to restart the USB device.

This pin is only used when it is necessary to improve the compatibility of such devices and does not normally need to be connected. There are 2 methods for controlling the power supply on/off. Choose one of them according to the actual situation when using it.

（1） Control 5V DCDC EN: Connect a 10K pull-up resistor to the VDD49 pin and connect the EN pin of the DCDC.



(2) Control the 5V power supply path NMOS gate: Pull up the 750K resistor to the HVCP pin and connect the external N-type MOSFET power transistor gate.



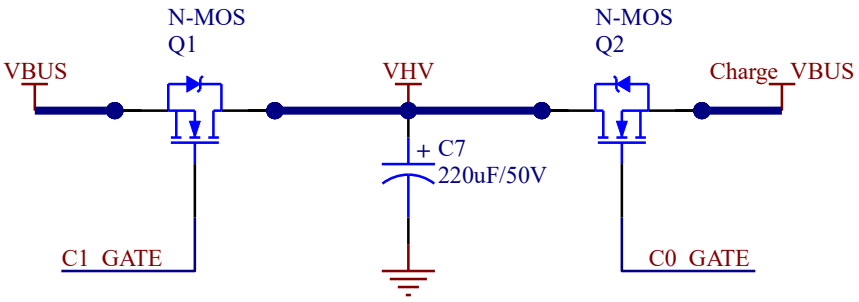
5.7 Power Control

The CH227F can reserve a portion of the power for use by the system's own equipment during power forwarding. The CH227F deducts 15W of power by default. Please contact our company if you need custom modifications.

5.8 Fast Role Exchange

When the power supply suddenly interrupts power supply, the CH227F will quickly switch power supply roles to achieve seamless power transmission, i.e., rapid role switching (FR_Swap). When using it, you need to add energy storage capacitors to the system power supply path according to actual needs to ensure voltage stability during the FR_Swap switching process.

When testing the evaluation board with a 5V 0.5A load, the capacitor should be no less than 220uF; for a 5V 1.5A load, the capacitor should be no less than 470uF. Actual results from board testing should be used as a reference. The connection diagram for the energy storage capacitor is shown in the figure below.


N-MOS
Q1
N-MOS
Q2
VBUS
VHV
Charge_VBUS
+ C7
220uF/50V
C1_GATE
C0_GATE

6. Parameters

6.1 CH227F Absolute Maximum Value (Critical or exceeding the absolute maximum value will probably cause the chip to work improperly or even be damaged)

Symbol	Parameter	Min.	Max.	Unit
T_A	Ambient temperature during operation	-40	85	℃
T_S	Ambient temperature during storage	-55	150	℃
V_{HVBUS}	Operating supply voltage	-0.4	32.0	V
V_{VDD49}	Supply voltage at pin VDD49	-0.4	6.5	V
V_{CCH}	Signal voltage of C1_CC1/C1_CC2 pins	-0.4	32.0	V
V_{GATEH}	Signal voltage of C0_GATE/C1_GATE/V5_EN pins	-0.4	40	V
V_{LVIO}	Signal voltage of CCL1/CCL2/CCGND and other pins	-0.4	6.5	V
V_{IOBC}	Signal voltage of DB/DC/S1B/S1C/S2B/S2C pins	-0.5	V_{VDD49}+0.4	V
V_{ESDCC}	HBM ESD tolerant voltage of C1_CC1/C1_CC2/HVBUS pins	6		KV
V_{ESDHV}	HBM ESD tolerant voltage of GATE/V5_EN/HVCP pin	2		KV
V_{ESDNO}	ESD tolerant voltage of the HBM human body model for the CCGND pin	0.8		KV
V_{ESDLV}	HBM ESD tolerant voltage of GPIO/CCL1/CCL2/VDD49 pins	2		KV
I_{IO1}	Continuous conduction current of a single I/O pin		30	mA
I_{IO8}	Pulse current with a duty cycle less than 1/8 of a single I/O pin		100	mA
I_{ALL}	Total current of all I/O pins		150	mA
PD	Maximum power consumption of the entire chip		500	mW
θ_{JA}	Packaging thermal resistance		100	℃/W

6.1 CH227P Absolute Maximum Value (Critical or exceeding the absolute maximum value will probably cause the chip to work improperly or even be damaged)

Symbol	Parameter	Min.	Max.	Unit
T_A	Ambient temperature during operation	-40	85	℃
T_S	Ambient temperature during storage	-55	125	℃
V_{VDD}	Operating supply voltage	-0.5	6.0	V
V_{VHV}	High voltage supply voltage	-0.5	25	V
V_{CN}	Voltage on VEN_A/VEN_B	-0.5	25	V
V_{IOCC}	Low voltage itself but can tolerant high voltage on pins CC0/CC1	-0.5	25	V
V_{IOHV}	Support high voltage on the VDET/PS_CTRL pin	-0.5	27	V
PD	Maximum power consumption of the entire chip		300	mW

6.3 CH227F Electrical Parameters (Test conditions: T_A = 25℃, V_{HVBUS} = 5V~28V)

Symbol	Parameter	Min.	Typ.	Max.	Unit

V_{HVBUS}	Supply voltage of HVBUS pin		4.7	5~28	29	V
V_{VDD49}	VDD49 pin LDO output voltage		4.7	4.9	5.1	V
$V_{HVBUS0V}$	Voltage threshold of HVBUS overvoltage monitoring OVP		31.5	33	34.5	V
I_{CP}	Load current of HVCP booster module				60	uA
V_{IL}	Low input voltage of SCL/SDA pin		0		0.8	V
V_{IH}	High input voltage of SCL/SDA pin		2.1		5	V
T_{IH}	OTP over-temperature monitoring threshold		110	130	150	℃
V_R	Voltage threshold for power-on reset		2.8	3.0	3.2	V
I_{VCONN}	C1_CC1/C1_CC2 pin VCONN load current				25	mA
I_W	Operating current with HVCP open but no load			0.8	2	mA
I_Q	Static current with HVCP OFF and idle	V_{HVBUS}< 3V		15	40	uA
		V_{HVBUS}≥ 5V		40	100	uA
V_{REFL}	Low reference voltage of V5_EN pin with 0.1V hysteresis		0.9	1.1	1.35	V
V_{REFH}	High reference voltage of V5_EN pin with 0.1V hysteresis		3.2	3.5	3.8	V
$I_{HVBUSDISC}$	Discharge current of HVBUS pin	V_{HVBUS} = 5V		25		mA
		V_{HVBUS} = 28V		30		mA
R_{PUSDA}	Built-in pull-up resistor of SDA pin		7	10	15	KΩ
R_d	Built-in Rd pull-down resistor of C1_CC pin	V_{CCH} ≥ 1.2V	4.2	5.1	6	KΩ
	Built-in Rd pull-down resistor of C0_CC pin	V_{HVBUS}≥ 2.8V				
R_{PU}	Built-in pull-up resistor of V5_EN pin		30	60	180	KΩ
R_{CP}	Built-in discharge resistor of HVCP pin		800	1200	1600	KΩ

6.4 CH227P Electrical Parameters (Test conditions: T_A = 25℃, V_{HV} = 3.3V~20V, V_{DD} = 3.3V)

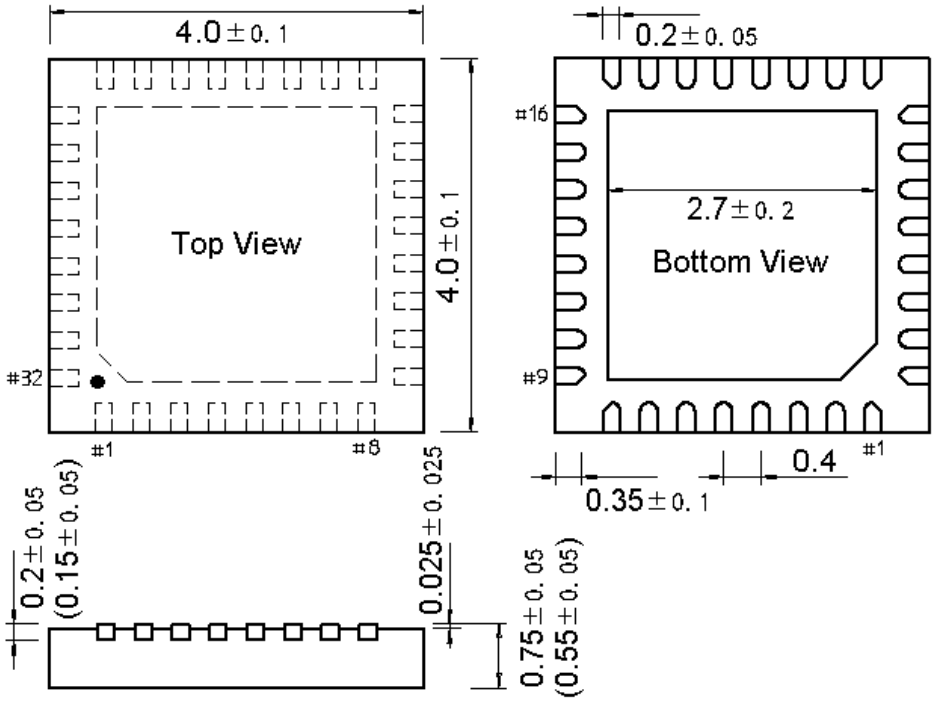
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{VHV}	Supply voltage of HV pin	2.7	5.0	22	V
V_{VDD}	VDD pin LDO output voltage	3.1	3.3	3.7	V
I_{CC}	Total supply current during operation		1.7	8	mA
V_{LDO}	Internal VDD power regulator LDO output voltage	3.2	3.3	3.4	V
I_{LDO}	Internal VDD power regulator LDO external load capability			4	mA
V_{VHVX}	VHV power supply overvoltage reset OVR protection voltage	25.5	27	28.5	V
V_R	VHV voltage threshold for power-on reset	2.3	2.55	2.7	V

7. Package Information

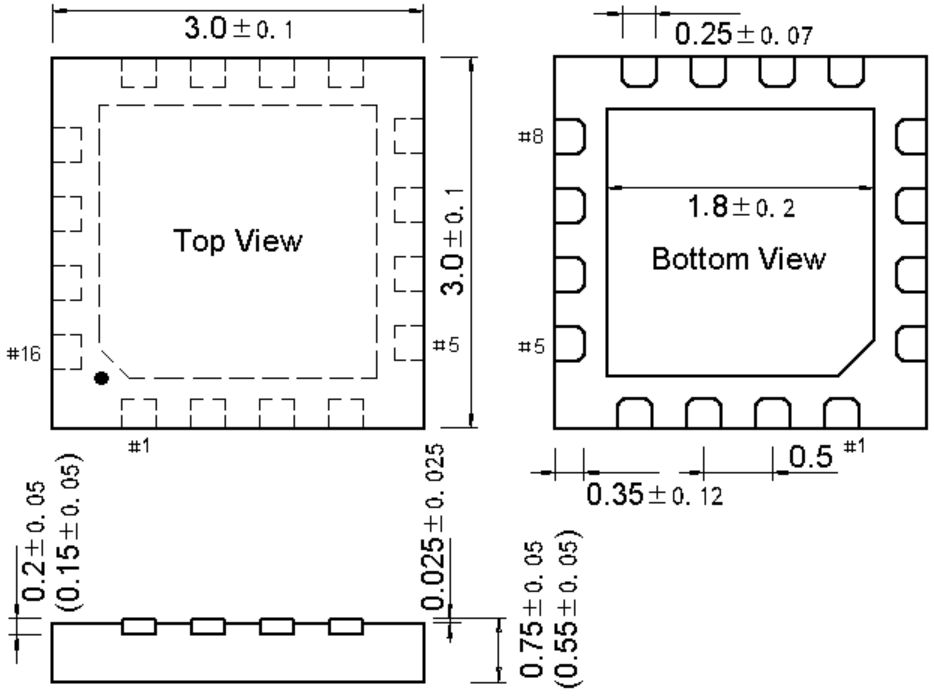
Note: Dimensions are marked in mm (millimeters)

The pin center spacing is the nominal value without error, and the dimensional error other than that is no more than ±0.2mm.

7.1 QFN32



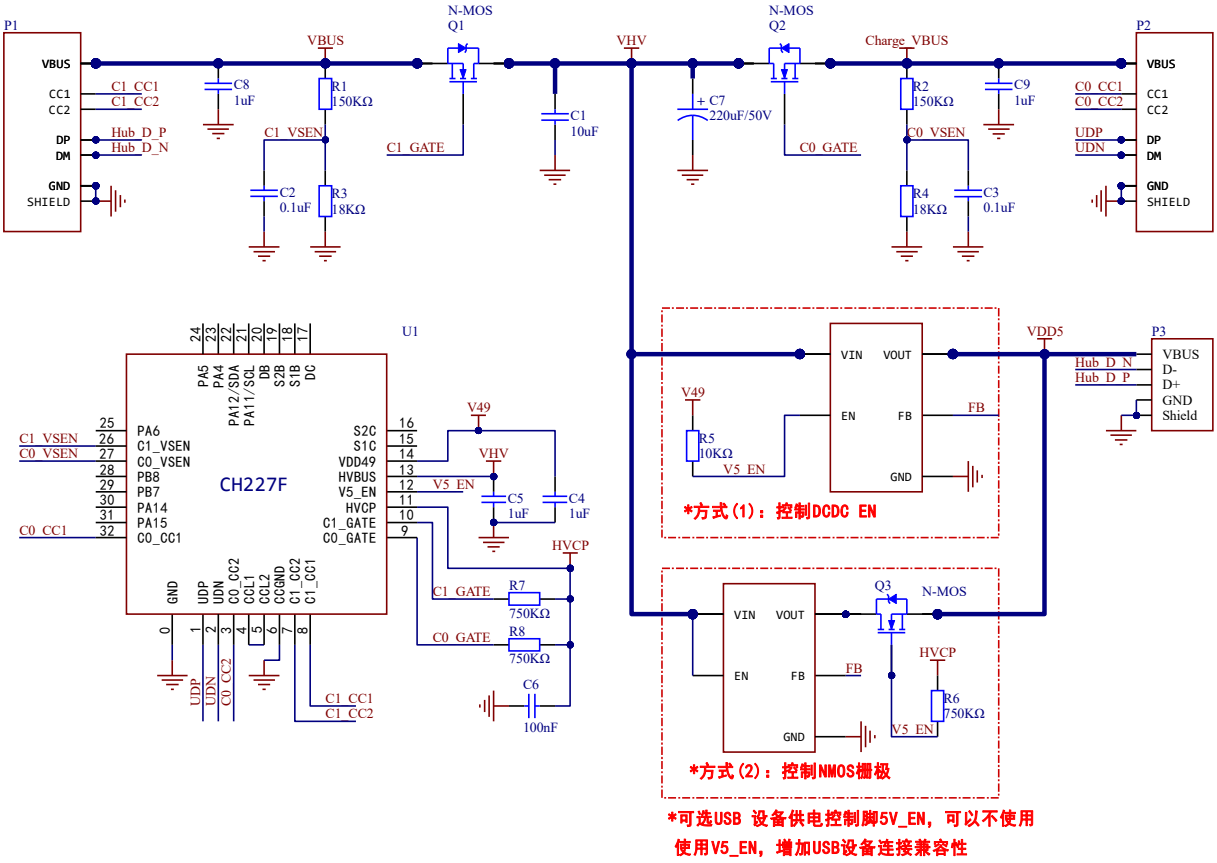
7.2 QFN16

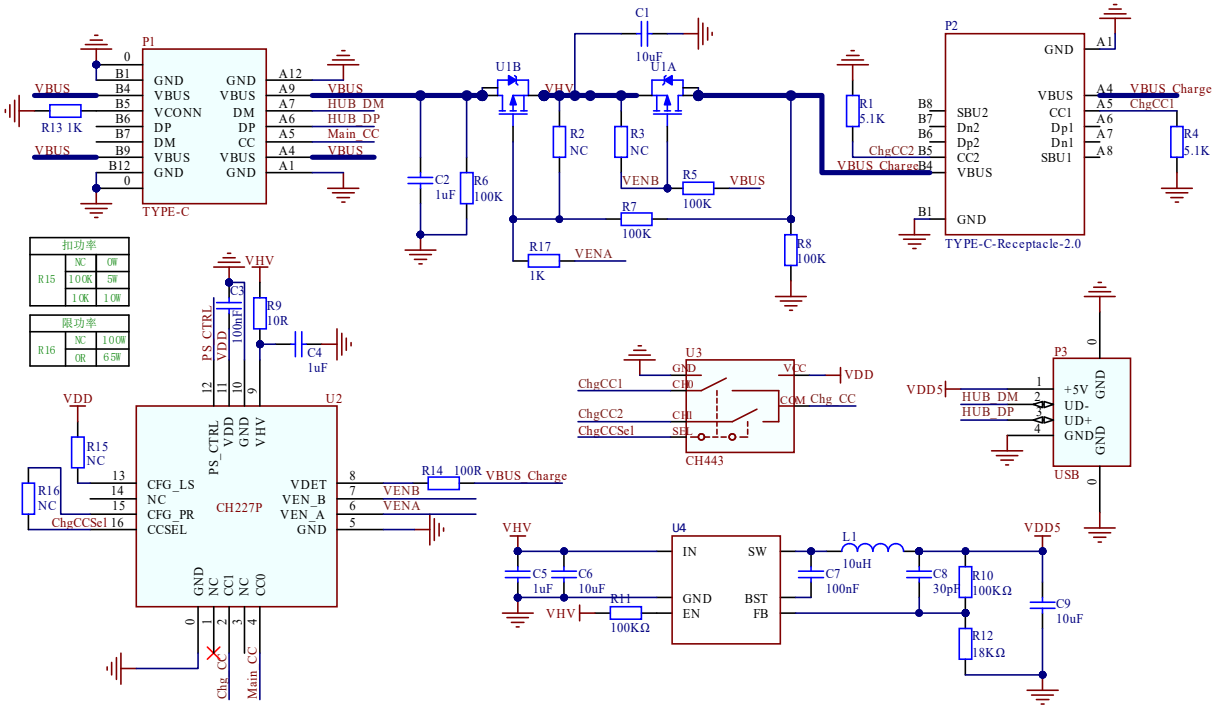


8. Applications

8.1 CH227F, dual-port non-blind plug solution

As shown in the figure below, P1 is the host-side Type-C port, and P2 is the power supply-side Type-C port. P3 is the host-side USB 2.0 port, and can also be connected to HUB chips such as CH334 to expand downstream ports. U1 is the CH227F chip, which supports PD charging transparent transmission. The boxed area is the V5_EN optional USB device power supply control pin. For specific usage methods, please refer to Section 5.6. C7 is an electrolytic capacitor supporting FR_Swap. For specific usage instructions, please refer to Section 5.8.



8.2 CH227P Application Reference Solution

As shown in the figure below, P1 is the host-side Type-C port, and P2 is the power supply-side Type-C port. P3 is the host-side USB 2.0 port, which can also be connected to CH334 or other HUB chips to expand downstream ports. U2 is CH227P chip, which supports PD charging transparent transmission.